REMARKS

Claims 1-24 are pending in the patent application ("Application").

Claim 1 and Claim 8 have been rejected.

Claims 15-24 have been allowed.

Claims 2-7 and Claims 9-14 have been objected to.

No claims have been amended.

Claims 1-24 remain in this Application.

Reconsideration of Claims 1-24 is respectfully requested.

Allowable Subject Matter

On Page 4 of the May 2, 2003 Office Action the Examiner allowed Claims 15-24. Also on Page 4 of the May 2, 2003 Office Action the Examiner objected to Claims 2-7 and 9-14 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicant respectfully accepts the allowance of Claims 15-24. The Applicant agrees that Claims 2-7 and Claims 9-14 recite allowable subject matter but respectfully disagrees that the base claims (Claim 1 and Claim 8) are not allowable.

Claim Rejections 35 U.S.C. § 103

On Page 4 of the May 2, 2003 Office Action the Examiner rejected Claim 1 and Claim 8 as being unpatentable over United States Patent No. 6,529,032 to *Cruickshank et al.* (hereafter "*Cruickshank*") in view of United States Patent No. 6,195,755 issued to *Webster et al.* (hereafter "*Webster*").

The Applicant respectfully traverses the rejection of Claim 1 and Claim 8. The Applicant respectfully requests the Examiner to withdraw the rejections of the above referenced claims in view of the Applicant's remarks concerning the prior art references.

During *ex parte* examinations of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of non-obviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re*

Grabiak, 769 F.2d 729, 733, 226 USPQ 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not be based on an applicant's disclosure. MPEP § 2142.

The Applicant respectfully submits that the Patent Office has not established a *prima facie* case of obviousness with respect to the Applicant's invention. The Applicant directs the Examiner's attention to Claim 1 and to Claim 8, which contain unique and novel limitations:

> 1. For use in an integrated circuit of the type comprising at least two power supply domains in which each power supply domain comprises at least one module powered by the same voltage level, an apparatus for blocking an output signal in a first power supply domain from being sent to a second power supply domain when said second power supply domain is in a low power mode. (Emphasis added).

> 8. For use in an integrated circuit of the type comprising at least two power supply domains in which each power supply domain comprises at least one module powered by the same voltage level, an apparatus for blocking an output signal in a first power supply domain from being received in a second power supply domain when said first power supply domain is in a low power mode. (Emphasis added).

Claim 1 is directed to an apparatus and method for blocking an output signal in a first power supply domain from being sent to a second power supply domain when the second power supply domain is in a low power mode. Claim 8 is directed to an apparatus and method for blocking an output signal from a first power supply domain from being received in a second power supply domain when the first power supply domain is in a low power mode. The Applicant's invention prevents the occurrence of "Back Drive" problems. As described in the specification (Pages 13-14) "Back Drive" problems are created when a data signal that is correctly sent from an active power supply domain is incorrectly received by an inactive power supply domain.

The Examiner stated "CRUICKSHANK discloses an apparatus for blocking an output signal in a first power supply domain (12) from being sent to a second power supply domain (14) when said second power supply domain is in a low power mode. CRUICKSHANK does not disclose an integrated circuit comprising two power supply domains." (May 2, 2003 Office Action, Paragraph 2, Page 2). The Applicant respectfully traverses the Examiner's assertion that *Cruickshank* discloses "an apparatus for blocking an output signal in a first power supply domain (12) from being sent to a second power supply domain (14) when said second power supply domain

is in a low power mode.

It is clear that *Cruickshank* does not disclose, teach or suggest an apparatus and method for blocking an output signal in a first power supply domain from being sent to a second power supply domain when the second power supply domain is in a low power mode. Specifically, *Cruickshank* states "When port 12 is in an output mode, denoted by switch 46 being closed, diode 34 begins to conduct current and effectively becomes a short circuit, shorting out shunt resistor 36, thereby allowing full output and diagnostic capabilities." (Emphasis added) (*Cruickshank*, Column 2, Lines 17-21). When port 12 of *Cruickshank* is in output mode (i.e., sending an output signal from port 12) diode 34 and shunt resistor 36 allow full output of the output signal. Therefore, *Cruickshank* does not teach the concept of blocking an output signal from being sent.

The same is true for output port 14. *Cruickshank* states that the operation of port 12 and the operation of port 14 are equivalent operations. (*Cruickshank*, Column 2, Lines 27-28). When port 14 sends an output signal, diode 40 and shunt resistor 42 allow full output of the output signal.

It is also clear that *Cruickshank* does not disclose, teach or suggest an apparatus and method for blocking an output signal from a first power supply domain from being received in a second power supply domain when the first power supply domain is in a low power mode. Specifically, *Cruickshank* states "When port 12 is in an input mode, denoted by switch 46 being open, an ON/OFF state of device 20 is reflected by a voltage across a preload resistor 50. The voltage across preload resistor 50, which is "read" by the controller or processor by being "shunted"

across shunt resistor 36, thereby bypassing diode 38, to input circuit 26." (*Cruickshank*, Column 2, Lines 21-26). Because input circuit 26 receives an input signal, an input signal from device 20 is not blocked in port 12.

Cruickshank also states "Diode 34 provides the backdrive protection. However, shunt resistor 36 which is mainly used to provide input feedback regarding the state of switch 46, also limits any currents entering the powered down controller to a level insufficient to repower the powered down controller of port 12, thereby avoiding any instability problems." (Emphasis added) (*Cruickshank*, Column 2, Lines 40-45). This shows that there are input currents that do enter port 12. That is, when port 12 of *Cruickshank* is in input mode it is clear that input signals are not blocked from entering port 12. The backdrive protection provided by the *Cruickshank* apparatus is not provided by blocking an input signal from being received in port 12, as disclosed and claimed by the Applicant.

There is no teaching, suggestion or even a hint in the *Cruickshank* reference concerning the Applicant's novel and unique concepts of (1) blocking an output signal in a first power supply domain from being sent to a second power supply domain when the second power supply domain is in a low power mode, and (2) blocking an output signal from a first power supply domain from being received in a second power supply domain when the first power supply domain is in a low power mode. A teaching or suggestion to make the Applicant's invention and a reasonable expectation of success is not found in the *Cruickshank* reference (or in any other prior art reference).

Therefore, the Applicant's invention is not *prima facie* obvious in view of the *Cruickshank* reference.

The Examiner stated "WEBSTER discloses an integrated circuit comprising two power supply domains (VPS1, VPS2)." (May 5, 2003 Office Action, Page 3, Lines 1-2). The Examiner further stated that it would have been obvious to one having ordinary skill in the art to combine the teachings of the *Webster* reference with the teachings of the *Cruickshank* reference. The Applicant respectfully traverses these assertions of the Examiner.

Webster discloses a power management apparatus for an integrated circuit in which "the power to a functional circuit contained in an integrated circuit is not completely removed, but decreased such that the functional circuit is placed in a reduced power mode of operation." (*Webster*, Column 2, Lines 50-53).

The functional circuit 99 of *Webster* is not equivalent to a power supply domain of the type described by the Applicant. *Webster's* definition of a functional circuit (*Webster*, Column 4, Lines 7-8) states that a functional circuit is "a means for performing a specified electronic function or group of electronic functions." Generally speaking, this definition of a functional circuit does not imply that the functional circuit comprises at least two power supply domains. There are many functional circuits that operate with only one power supply.

Webster shows a Power In Net No. 1 (40) of functional circuit 99 that may be considered analogous to a power supply domain. In the prior art circuit shown in Figure 1 of *Webster* Power In

Net No. 1 (40) receives power from Power In Pad No. 1 (20). *Webster* also shows a plurality of "Power In Net" modules (up to Power In Net No. P (41)) within functional circuit 99. In the prior art circuit shown in Figure 1 of *Webster* Power In Net No. P (41) receives power from Power In Pad No. P (21).

In the apparatus of *Webster* shown in Figures 2 through 4 *Webster* places a "variable power source" (VPS) circuit between each "Power In Pad" (located at the edge of integrated circuit 201, 202 and 203) and its corresponding "Power In Net" (located in functional circuit 99). For example, Variable Power Source No. 1 (60) is located between Power In Pad No. 1 (20) and Power In Net No. 1 (40). Variable Power Source No. 1 (60) converts a first voltage level to a second voltage level and provides the second voltage level to Power In Net No. 1 (40) (*Webster*, Column 11, Lines 54-65).

Similarly, Variable Power Source No. P (61) is located between Power In Pad No. P (21) and Power In Net No. P (41). Variable Power Source No. P (61) converts a first voltage level to a second voltage level and provides the second voltage level to Power In Net No. P (41) (*Webster*, Column 11, Line 66 to Column 12, Line 10). *Webster* controls the plurality of Variable Power Sources with Power Control Pad 26.

Each Power In Net in functional circuit 99 is coupled to its own corresponding Power In Pad through its own corresponding Variable Power Source. That is, each Variable Power Source is exclusively coupled to its own Power In Net. For example, there is no connection between Variable

Power Source No. 1 (60) and Power In Net No. P (41).

Furthermore, *Webster* does not disclose any communication between the various Power In Net modules in functional circuit 99. There is no mention of any communication between Power In Net No. 1 (40) and Power In Net No. P (41). Therefore, it is clear that *Webster* is completely silent concerning the concept of sending a signal from a first power supply domain to a second power supply domain. Accordingly, there is nothing in *Webster* that discloses, teaches or suggests the concept of sending signals (or blocking signals) between two power supply domains. There is nothing in *Webster* than discloses, teaches or suggests the concept of sending signals (or blocking signals) between two power supply domains based upon the state of the power level of one of the two power supply domains. Nothing in the *Webster* reference recites the unique and novel claim limitations of Claim 1 and Claim 8 of the present patent application.

The Applicant respectfully traverses the Examiner's assertion that it would have been obvious to combine the *Cruickshank* reference with the *Webster* reference. Under the applicable patent law, there must be some teaching, suggestion or motivation to combine the *Cruickshank* reference and the *Webster* reference. "When a rejection depends on a combination of prior art references, there must be some teaching, or motivation to combine the references." *In re Rouffet*, 149 F.3d 1350, 1355-56, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998). "It is insufficient to establish obviousness that the separate elements of an invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the references." *Arkie Lures, Inc. v. Gene Larew Tackle, Inc.*, 119 F.3d

953, 957, 43 USPQ2d 1294, 1297 (Fed. Cir. 1997). The Applicant respectfully submits that there exists no teaching, suggestion or motivation in the prior art to combine the teachings of the *Cruickshank* reference and the teachings of the *Webster* reference. The *Cruickshank* reference discloses two I/O controller ports, 12 and 14. In the *Webster* reference the I/O port switches (I/O Switch No.1 (62) to I/O Switch No. K (63)) are separate from the Variable Power Sources (VPS No. 1 (60) to VPS No.P (61)). This fact shows that the *Webster* reference teaches away from combining the *Cruickshank* reference with the *Webster* reference.

When two references are combined the combination of the references must teach or suggest all the claim limitations. In the present case, even if the *Cruickshank* reference were combined with the *Webster* reference, the combination of the *Cruickshank* reference and the *Webster* reference would not teach, suggest or even hint at the Applicant's invention. This is because neither the *Cruickshank* reference nor the *Webster* reference teaches, suggests, or even hints at the Applicant's concepts of (1) blocking an output signal in a first power supply domain from being sent to a second power supply domain when the second power supply domain is in a low power mode, or (2) blocking an output signal from a first power supply domain from being received in a second power supply domain when the first power supply domain is in a low power mode. The Applicant therefore respectfully submits that the rejections of Claim 1 and Claim 8 under 35 U.S.C. §103(a) combining the *Cruickshank* reference and the *Webster* reference should be withdrawn.

The Applicant respectfully submits that because Claim 1 and Claim 8 both recite patentable subject matter, the objections with respect to Claims 2-7 and Claims 9-14 should be withdrawn.

The Applicant respectfully submits that Claims 1-24 are all patentable over the *Cruickshank* reference and the *Webster* reference whether taken individually or in combination. The Applicant respectfully requests that the rejections of Claim 1 and Claim 8 be withdrawn and that Claims 1-24 all be passed to issue.

The Applicant's attorney has made the amendments herein and the arguments set forth above in order to place this Application in condition for allowance. In the alternative, the Applicant's attorney is making the same to properly frame the issues for appeal. In this Amendment, the Applicant makes no admission concerning any now moot rejection or objection, and affirmatively denies any position, statement or averment of the Examiner that was not specifically addressed herein.

SUMMARY

The Applicant respectfully requests consideration and allowance of the above claims. If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this Amendment or credit any overpayment to National Semiconductor Deposit Account No. 14-0448.

Respectfully submitted,

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